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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,569	04/24/2001	Joseph E. Eckelman	POU92001050US1	5426

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,569	ECKELMAN ET AL.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☒ Claim(s) *1-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because:

- Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action.
- Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

- The abstract is more than 150 words and therefore is objected to. Applicant is reminded of the proper language and format for an abstract of the disclosure.

> ***The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.***
>
> ***The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as,***

"The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

- On page 1, line 11 of the specification, the comma after "High speed" needs to be omitted.
- On page 1, line 15 of the specification, the comma after "Manufacturing yield" needs to be omitted.
- On page 14, lines 5-10 of the specification, the extra space between paragraphs should be omitted.
- The lengthy specification has not been checked to the extent necessary to determine the presence of all possible grammatical errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Claim Objections

Claim 1 is objected to because of the following informalities:

- The term "consisting" in the second paragraph is misspelled.
- The phrase "...not only..." in the third paragraph needs to be omitted. This phrase is normally used in conjunction with "but" "addition" etc. and since these terms do not follow in the claim language it is grammatically improper to use "...not only..."
- Applicant is hereby notified that claim 1 is a hybrid claim because it includes a method and apparatus.

  An application containing a hybrid claim wherein, for instance, a product is defined merely in terms of the process for producing it. See MPEP § 705.01(e), situation (A).

Claims 1-7 are objected to because of the following informalities:

- The claims tell a story instead of incorporating limitations therein.
- There is lack of indentations in the claims.

Appropriate correction is required.

Claim 3 is objected to because of the following informalities:

- The term "identifying" in the first paragraph is misspelled.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "N" is not defined in the claim language and therefore, for the purposes of rejection it can be construed to be anything. Furthermore, ambiguity is created because if, for example, N is 0 then no actual "skipping" is performed. Therefore, the Applicants are advised to give N a specific value or a range of values to make the claim language definite.
- Claims 2-7 dependent from independent claim 1 and inherently include limitations therein and therefore are rejected as well.
- Claim 2 recites the limitation "...existing address registers for providing data..." in line 2. There is insufficient antecedent basis for this limitation in the claim since claim 2 depends on claim 1 and in claim 1 there is no indication of any "...existing address registers for providing data..."

- Claim 3 recites the limitation "result vector" in lines 1-2. There is insufficient antecedent basis for this limitation. However, the Examiner will assume "result vector" to be "failed result vector." Applicants are requested to make necessary changes.
- Claim 4 recites the limitation "the skip counter" in line 5. There is insufficient antecedent basis for this limitation. However, the Examiner will assume "the skip counter" to be "the programmable skip counter." Applicants are requested to make necessary changes.
- Claim 7 recites the limitation "said supplemental address register" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.
- Claim 7 recites the limitation "said 'Record first fail'..." in lines 7-8. There is insufficient antecedent basis for this limitation. However, the Examiner will assume "said 'Record first fail'..." to be "said 'Record first fail' mode..." Applicants are requested to make necessary changes.
- Claim 7 recites the limitation "the LSSD registers" in lines 10-11. There is insufficient antecedent basis for this limitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui (USPN 6594788B1) further in view of Sato (USPN 5790559).

As per claim 1, Yasui substantially teaches (title and abstract) a method of analyzing a repair of failure memory cell in a memory, which is capable of searching a must-repair of a memory at high speed and of performing a simulation process for relieving a must-repair at high speed at the time point when it has been detected. There are provided a row address failure number counter/memory for counting the number of failure memory cells on each row address in the row address direction and storing it and a column address failure number counter/memory for counting the number of failure memory cells on each column address in the column address direction and storing it. The stored value in either one counter/memory is read out and the number of failure memory cells on each address is compared with the number of spare lines. The state that the number of failure memory cells on each address is greater than the number of spare lines is determined to be a must-repair, and a simulation process for relieving the failure is executed at the time point when the must-repair has been detected. Furthermore, Yasui teaches (Figure 5) a block diagram showing a schematic configuration of memory testing apparatus having failure relief analyzer. This memory testing apparatus TES comprises a main controller 111, a pattern generator 112, a timing generator 113, a waveform formatter 114, a logical comparator 115, a driver 116, an analog level comparator 117, a failure analysis memory 118, a failure relief analyzer 120, a logical amplitude reference voltage source 121, a comparison reference voltage source 122 and a device power source 123. The main controller 111 is generally constituted by a computer system in which a test program PM created by a user

(programmer) is loaded in advance, and the control of the entire memory testing apparatus is performed in accordance with the test program PM. This main controller 111 is connected, via a tester bus BUS, to the pattern generator 112, the timing generator 113, the failure analysis memory 118, the failure relief analyzer 120 and the like. The logical amplitude reference voltage source 121, the comparison reference voltage source 122 and the device power source 123 are also connected to the main controller 111. Yasui teaches that before starting the test of the IC memory, various kinds of data are set by the main controller 111. After the various kinds of data have been set, the test of the IC memory is started. When the main controller 111 issues a test starting command to the pattern generator 112, the pattern generator 112 starts to generate a pattern. The pattern generator 112 supplies a test pattern data to the waveform formatter 114 in accordance with the test program PM. On the other hand, the timing generator 113 generates a timing signal (clock pulses) for controlling operation timings of the waveform formatter 114, the logical comparator 115 and the like.

Yasui does not explicitly teach, "...skip up to an 'Nth' failing cell and recording the failure of the subsequent 'Nth + 1' fail."

However, Sato, in an analogous art, teaches (abstract) a memory unit for storing failure data of a semiconductor memory under test comprises a plurality of interleaved DRAMs. A buffer memory temporarily stores failure data to be stored into the DRAMs and addresses thereof. The DRAMs are associated respectively with storage controllers which store failure addresses whose row addresses correspond to the DRAMs, among inputted failure addresses, into buffer memories associated respectively with the DRAMs. Write controllers are associated respectively with the DRAMs, for reading the failure data from the buffer memories and writing

the failure data into the DRAMs in a high-speed write mode. In particular, Sato teaches (col. 8-9, lines 42-68 and 1-19) each of the memory controllers comprise a refresh timer for generating a refresh request signal, a read/write trigger generator for being supplied with the failure storage signal and a one-address storage signal which is outputted each time the storage of failure data into the corresponding DRAM is finished, turning on a read/write operation flag and outputting a read/write trigger signal to start a read/write mode of operation of the DRAM when a refresh operation flag is turned off and the read/write request signal is supplied, a refresh trigger generator responsive to the refresh request signal for turning on the refresh operation flag and outputting a refresh start signal when the failure storage operation flag is turned off, a circuit for effecting operation modes of the DRAM, a timing generation memory for storing in advance timing data to refresh the DRAM and store the failure data into the DRAM, a program counter for generating address pointers for the timing generation memory, a sequence memory for storing sequence data to increment, decrement, and hold data in the program counter, the sequence memory having address pointers generated by the program counters, an operation mode register for storing start addresses of the timing generation memory and the sequence memory in each of the operation modes, and a sequence controller for operating the program counter according to the sequence data outputted from the sequence memory in response to the read/write trigger signal outputted from the read/write trigger generator or the refresh start signal outputted from the refresh trigger generator. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the programmable timing capabilities of Sato into the failure data collection of Yasui. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would

have recognized that by using a programming means to collect failure data of particular interest would reduce testing time since the most vulnerable cells may be tested first.

As per claims 2 and 3, Yasui substantially teaches, in view of above rejections, (Figure 7) that each storage area 2 has a memory cell array MCA in which memory cells have been arrayed in a matrix manner of rows and columns, and in addition to the memory cell array MCA, is provided with a desired number of row spare lines SR and a desired number of column spare lines SC formed in the row address direction ROW and in the column address direction COL along the periphery of the memory cell array MCA, respectively. These spare lines SR and SC are provided for the purpose of relieving failure memory cells, and serve to change a memory under test that has been determined to be a defective or failure article to a non-defective or pass article by electrically replacing the detected failure memory cells in the storage area 2 with those spare lines. Further, in this example, a case is shown where two row spare lines SR are disposed along one side of the row address direction of the memory cell array MCA and two column spare lines SC are disposed along one side of the column address direction of the memory cell array MCA, respectively. The number of failure memory cells that can be relieved by the spare lines orthogonal to address line directions in the storage area 2 is restricted by the number of the spare lines SR formed in the row address direction ROW and the number of spare lines SC formed in the column address direction COL. For this reason, after the test is completed, at first the number of failure memory cells is obtained for each storage area 2, and row address lines and column address lines on which these failure memory cells are present are located for each storage area 2 to determine whether or not those failure memory cells on

those address lines can be relieved by the spare lines orthogonal to their respective address lines.

As per claims 4-7, Sato substantially teaches, in view of above rejections, (col.7, lines 5-68) the memory controllers comprises a refresh timer for generating a refresh request signal, a failure storage trigger generator for being supplied with the failure storage signal and a one-address storage signal which is outputted each time the storage of failure data into the corresponding DRAM is finished, turning on a failure storage operation flag and outputting a failure storage trigger signal to start storing the failure data from the buffer memory means into the DRAM when a refresh operation flag is turned off and a count of the failure storage signal and a count of the one-address storage signal disagree with each other, a refresh trigger generator responsive to the refresh request signal for turning on the refresh operation flag and outputting a refresh start signal when the failure storage operation flag is turned off, a read/modify/write circuit for effecting the read/modify/write mode to store failure data into the DRAM, a timing generation memory for storing in advance timing data to refresh the DRAM and store the failure data into the DRAM, a program counter for generating address pointers for the timing generation memory, a sequence memory for storing sequence data to increment, decrement, and hold data in the program counter, the sequence memory having address pointers generated by the program counters, and a sequence controller for operating the program counter according to the sequence data outputted from the sequence memory in response to the failure storage trigger signal outputted from the failure storage trigger generator or the refresh start signal outputted from the refresh trigger generator.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yasui teaches a method of analyzing a repair of failure memory cell in a memory, which is capable of searching a must-repair of a memory at high speed and of performing a simulation process for relieving a must-repair at high speed at the time point when it has been detected. Sato teaches a memory unit for storing failure data of a semiconductor memory under test comprises a plurality of interleaved DRAMs. Applicants are further invited to read/review additional pertinent prior arts that have been included herein.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
March 3, 2004

Guy J. Lamarre for

Albert DeCady
Primary Examiner